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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/303,669	05/03/1999	STEFANOS SIDIROPOULOS	RMBS.002	8670

7590 04/23/2002

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EXAMINER	
FAN, CHIEH M	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 04/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Form PTO 948 (Rev. 8-98) U.S. DEPARTMENT OF COMMERCE - Patent and Trademark Office Application No. 09/303,669

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 5/3/99 are:

A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.

B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be sumitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color.
   ____ Color drawings are not acceptable until petiton is granted. Fig(s) ____
   ____ Pencil and non black ink not permitted. Fig(s) ____
2. PHOTOGRAPHS. 37 CFR 1.84 (b)
   ____ 1 full-tone set is required. Fig(s) ____
   ____ Photographs not properly mounted (must use brystol board or photographic double-weight paper). Fig(s) ____
   ____ Poor quality (half-tone). Fig(s) ____
3. TYPE OF PAPER. 37 CFR 1.84(e)
   ____ Paper not flexible, strong, white, and durable. Fig(s) ____
   ____ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) ____
   ____ Mylar, velum paper is not acceptable (too thin). Fig(s) ____
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
   ____ 21.0 cm by 29.7 cm (DIN size A4)
   ____ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   ____ All drawing sheets not the same size. Sheet(s) ____
   ____ Drawings sheets not an acceptable size. Fig(s) ____
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:
   Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm SIZE: A4 Size
   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm SIZE: 8 1/2 x 11
   Margins not acceptable. Fig(s) 1, 3, 5, 6, 9
   ✗ Top (T) ✗ Left (L)
   ____ Right (R) ____ Bottom (B)
6. VIEWS. 37 CFR 1.84(h)
   REMINDER: Specification may require revision to correspond to drawing changes.
   Partial views. 37 CFR 1.84(h)(2)
   ____ Brackets needed to show figure as one entity. Fig(s) ____
   ____ Views not labeled separately or properly. Fig(s) ____
   ____ Enlarged view not labeled separetely or properly. Fig(s) ____
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
   ____ Hatching not indicated for sectional portions of an object. Fig(s) ____
   ____ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) ____
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   ____ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) ____
9. SCALE. 37 CFR 1.84(k)
   ____ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) ____
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(i)
    ____ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s) ____
11. SHADING. 37 CFR 1.84(m)
    ____ Solid black areas pale. Fig(s) ____
    ____ Solid black shading not permitted. Fig(s) ____
    ____ Shade lines, pale, rough and blurred. Fig(s) ____
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
    ____ Numbers and reference characters not plain and legible. Fig(s) ____
    ____ Figure legends are poor. Fig(s) ____
    ____ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s) ____
    ____ English alphabet not used. 37 CFR 1.84(p)(2) Figs ____
    ____ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) ____
13. LEAD LINES. 37 CFR 1.84(q)
    ____ Lead lines cross each other. Fig(s) ____
    ____ Lead lines missing. Fig(s) ____
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
    ____ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) ____
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    ____ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) ____
16. CORRECTIONS. 37 CFR 1.84(w)
    ____ Corrections not made from prior PTO-948 dated ____
17. DESIGN DRAWINGS. 37 CFR 1.152
    ____ Surface shading shown not appropriate. Fig(s) ____
    ____ Solid black shading not used for color contrast. Fig(s) ____

COMMENTS

REVIEWER Q.D DATE 6/22/99 TELEPHONE NO. ____

ATTACHMENT TO PAPER NO. ____

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities--37 CFR 1.85

File new drawings with the changes incorporated therein. The application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application, should be placed on the back of each sheet of drawings in accordance with 37 CFR 1.84(c). Applicant may delay filing of the new drawings until receipt of the Notice of Allowability (PTOL-37). Extensions of time may be obtained under the provisions of 37 CFR 1.136. The drawing should be filed as a separate paper with a transmittal letter addressed to the Drawing Processing Branch.

2. Timing for Corrections

Applicant is required to submit **acceptable** corrected drawings within the three-month shortened statutory period set in the Notice of Allowability (PTOL-37). If a correction is determined to be unacceptable by the Office, applicant must arrange to have acceptable corrections resubmitted within the original three-month period to avoid the necessity of obtaining an extension of time and paying the extension fee. Therefore, applicant should file corrected drawings as soon a possible.

Failure to take corrective action within set (or extended) period will result in **ABANDONMENT** of the Application.

3. Corrections other than Informalities Noted by the Drawing Review Branch on the Form PTO-948

All changes to the drawings, other than informalities noted by the Drawing Review Branch, **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Office Action Summary	Application No. 09/303,669	Applicant(s) SIDIROPOULOS, STEFANOS
	Examiner Chieh M Fan	Art Unit 2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10,11 and 26-29* is/are rejected.

7)☒ Claim(s) *5-9,12-25,30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 3 and 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: logic NAND gate 607 (see page 17, line 9). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 5-9, 11-15, 17-25 and 31 are objected to because of the following informalities:

Regarding claims **5-9**, claim 5 recites the limitations of "a third supply voltage" and "a fourth supply voltage", but never recites a first supply voltage and a second supply voltage. Therefore, the following changes should be made:

(1) In claim 5, lines 3-4, "a third supply voltage" should be changed to "a first supply voltage";

(2) In claim 5, line 5, "a fourth supply voltage" should be changed to "a second supply voltage";

(3) In claim 6, line 1, "a second load" should be "the second load";

(4) In claim 6, line 3, "the third supply voltage" should be changed to "the first supply voltage";

(5) In claim 6, lines 3-4, "the fourth supply voltage" should be changed to "the second supply voltage";

(6) In claim 8, line 4, "the first and second load transistor" should be "the first and second load transistors";

(7) In claim 8, lines 4-5, "a fifth supply voltage" should be changed to "a third supply voltage";

(8) In claim 8, lines 6-7, "a sixth supply voltage" should be changed to "a fourth supply voltage";

(9) In claim 8, lines 9-10, "the sixth supply voltage" should be changed to "the fourth supply voltage";

(10) In claim 9, line 3, "the fifth supply voltage" should be changed to "the third supply voltage";

(11) In claim 9, line 3, "the sixth supply voltage" should be changed to "the fourth supply voltage";

Regarding claim **11**, the examiner suggests the following changes to improve the readability.

(1) In line 3, "a logic gate" should be changed to "a first logic gate";

(2) In line 3, "the logic gate" should be changed to "the first logic gate";

(3) In line 5, "a logic gate" should be changed to "a second logic gate";

(4) In line 5, "the logic gate" should be changed to "the second logic gate".

Regarding claims **12-15**, the limitation "a supply voltage" in line 3 of claim 12 should be changed to "a first supply voltage", since the limitation "a supply voltage" has been used to represent the voltage input to the delay line in claim 1 (see line 3 of claim 1). Similarly, "the supply voltage" in lines 9 and16 of claim 12 and in line 1 of claim 13 should be changed to "the first supply voltage".

Regarding claims **17-25**, claims 17-25 recite the limitations "a first supply voltage", "a third supply voltage", "a fourth supply voltage", "a fifth supply voltage", "a sixth supply voltage", but never recite <u>a second supply voltage</u>. The examiner suggests changing the limitation "a supply terminal" in the last line of claim 17 to "a second supply voltage" to fill the gap. Otherwise, the applicant needs to change "a third supply voltage" to "a second supply voltage", "a fourth supply voltage" to "a third supply voltage", and so forth. Furthermore, the following informalities need to be changed:

(1) In claim 17, line 15, "a non-inverting" should be changed to "an inverting";

(2) In claim 17, line 21, "a bias voltage" should be "the bias voltage";

(3) In claim 19, lines 3-4, "the fourth supply voltage is a ground voltage" should be changed to "a fourth supply voltage coupled to the bias transistor, wherein the fourth supply voltage is a ground voltage" to provide a proper antecedent basis for "the fourth supply voltage";

(4) In claim 20, lines 1-2, "the first load transistor" should be "the first transistor";

(5) In claim 20, line 2, "the second load transistor" should be "the second transistor";

(6) In claim 20, line 3, "the first and second load transistor" should be changed "the first and second transistors";

(7) In claim 22, line 4, "the second current mirror" should be "the second current mirror load circuit";

(8) In claim 22, line 7, "the third load transistor" should be "the first load transistor";

(9) In claim 22, line 10, "the fourth load transistor" should be "the second load transistor";

(10) In claim 24, line 3, "the second current mirror bias" should be changed to "a second current mirror bias".

Regarding claim **31**, the limitation "having an output" in line 2 should be changed to "having a first input, a second input, and an output" to provide proper antecedent basis for the limitations of "the first input" and "the second input" in line 4 and line 5, respectively. Further, "the bias voltage" in line 7 should be changed to "the bias signal".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Tamura et al. (US Patent 6,247,138, "Tamura" hereinafter).

Regarding claim **26**, Tamura discloses a method of generating a supply voltage ("CS" in Fig. 44, note that CS is a control voltage, see bottom of Fig. 45) for use in clock compensation circuitry (301 in Fig. 44), the clock compensation circuitry includes a plurality of delay elements in a delay line (311 in Fig. 4) and receives a clock signal ("CKr" in Fig. 44), the method comprising:

providing a supply voltage to a common source electrode of the plurality of delay elements ("CS" input to 311 in Fig. 44, also see Fig. 45 for the details of each of the delay element "D");

providing a delayed clock signal using the delay line ("CKin" in Fig. 44) , the delayed clock signal having a time delay with respect to the clock signal (as shown in Fig. 44, "CKin" is obtained by delaying "CKr");

detecting a delay skew between the delayed clock signal and the clock signal (312 in Fig. 44);

converting the delay skew to a voltage signal wherein the voltage signal is proportional to the delay skew (131 in Fig. 44, especially "Vco" output from 131 in Fig. 44); and

tracking the voltage signal using an amplifier (132 in Fig. 44) to generate the supply voltage ("CS" in Fig. 44).

Regarding claim **27**, Tamura also teaches that the delayed clock signal ("CKin" in Fig. 44) is provided by propagating the clock signal ("CKr" in Fig. 44) through the plurality of delay elements ("D" within 311 in Fig. 44) and tapping an output of one of the delay elements from the plurality of delay elements ("CKin" is output from the last delay element of 311 in Fig. 44).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US Patent 6,247,138, "Tamura" hereinafter) in view of Lai (US Patent 5,339,009).

Regarding claim **1**, Tamura discloses a clock alignment circuit comprising:

a delay line having a plurality of delay elements (311 in Fig. 44), wherein each delay element of the plurality of delay elements includes a supply electrode to receive a supply voltage ("CS" input to 311 in Fig. 44, also see Fig. 45 for the details of each of the delay element "D", also note that "CS" is a control voltage, see bottom of Fig. 45), to generate a delayed clock signal ("CKin" in Fig. 44) with respect to a reference clock signal ("CKr" in Fig. 44);

a comparator (312 in Fig. 44), coupled to the delay line, to compare the delayed clock signal and the reference clock signal and to output delay differential information ("UP" and "DN" output from 312 in Fig. 44), wherein the delay differential information is representative of a correction information between the reference clock signal and the delayed clock signal;

charge pump circuitry (131 in Fig. 44), coupled to the comparator, to convert the delay differential information to a control signal ("Vco" output from 131 in Fig. 44), wherein the control signal is proportional to the delay differential information;

an amplifier (132 in Fig. 44) coupled to the charge pump circuitry, wherein the amplifier includes:

a first input ("+" terminal of 132 in Fig. 44) to receive the control signal;

a second input ("-" terminal of 132 in Fig. 44) to receive a feedback signal; and

an output (output of 132 in Fig. 44) to provide the supply voltage and the feedback signal.

Tamura does not teach a capacitor coupled between the supply voltage and a secondary power supply (i.e., a ground voltage).

However, the use of a capacitor to bypass or filter undesired high-frequency noise is known in the art. Lai teaches a capacitor (64 in Fig. 2) coupled to the output of an amplifier (54 in Fig. 2) and a secondary power supply to bypass or filter unwanted noise (col. 6, lines 19-23) of the signal output from the amplifier.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to couple a capacitor between the supply voltage and a secondary power supply in the circuit of Tamura to bypass or filter the undesired noise in the supply voltage before the supply voltage is supplied to the delay elements of the delay line, and consequently to generate a more stable delayed clock signal from the delay line.

Regarding claim **2**, Tamura teaches the claimed limitation that the first input is a non-inverting input (see "+" terminal of 132 in Fig. 44) and the second input is an inverting input (see "-" terminal of 132 in Fig. 44).

Regarding claim **4**, Tamura teaches the claimed limitation that the delay line includes a plurality of inverter delay elements (Fig. 45 and col. 32, lines 47-48).

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. in view of Lai as applied to claim 1 above, and further in view of Dally et al. (*Digital Systems Engineering*, Cambridge, 1998, pp. 589-607).

As applied to claim 1 above, Tamura in view of Lai discloses the claimed invention including each of the delay elements in the delay line is an inverter delay element (col. 32, lines 47-48), but fails to disclose that the delay line includes a plurality of differential delay elements.

However, Dally et al. teaches that a differential delay element has better supply-noise rejection than an inverter delay element (the last two lines on page 593 through the first four lines on page 594).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the inverter delay elements in the delay line of Tamura in view of Lai with differential delay elements, since the use of differential delay elements has the advantage of higher power supply noise immunity than the use of inverter delay elements.

9. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. in view of Lai as applied to claim 1 above, and further in view of Sidiropoulos et al. ("A semidigital Dual Delay-Locked Loop", *IEEE Journal of Solid-State Circuits*, vol. 21, no. 11, Nov. 1997, pp. 1683-1692, provided in IDS filed on 6/28/99, PTO Paper#2).

Tamura in view of Lai teaches the claimed invention, as applied to claim 1 above, but fails to teach that the comparator includes a first pulse generator, a second pulse generator and a latch circuit as recited in claims 10 and 11, wherein the comparator corresponds to the comparator shown in Fig. 6 of the instant application. The first pulse generator corresponds to element 601 in Fig. 6. The second pulse generator corresponds to element 602 in Fig. 6. The latch circuit corresponds to element 603 in Fig. 6.

On the other hand, Sidiropoulos et al. discloses an identical phase comparator (see Fig. 7) with the phase comparator shown in Fig. 6 of the instant application. The phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock (page 1688, left column, lines 3-5). The phase comparator of Sidiropoulos et al. and the phase comparator shown in Fig. 6 of the instant application have exactly the same structure and perform the same function (i.e., phase comparison between the delayed clock signal and the reference clock signal).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the phase comparator taught by Sidiropoulos et al.

in place of the phase comparator of Tamura in view of Lai, since the phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock.

10. Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US Patent 6,247,138, "Tamura" hereinafter) in view of Sidiropoulos et al. ("A semidigital Dual Delay-Locked Loop", *IEEE Journal of Solid-State Circuits*, vol. 21, no. 11, Nov. 1997, pp. 1683-1692, provided in IDS filed on 6/28/99, PTO Paper#2).

Regarding claim **28**, Tamura teaches the claimed invention (see the rationale applied to claim 26 above), but fails to teach that the step of detecting the delay skew includes the steps of generating a first pulse, generating a second pulse, setting a latch circuit using the first pulse, and resetting the latch circuit using the second pulse, wherein all steps are performed by the phase comparator shown in Fig. 6 of the instant application. The step of generating a first pulse is performed by the first pulse generator 601 in Fig. 6. The step of generating a second pulse is performed by the second pulse generator 602 in Fig. 6. The step of setting a latch circuit using the first pulse is achieved by sending the pulse 610 to the latch circuit 603. The step of resetting the latch circuit using the second pulse is achieved by sending the pulse 611 to the latch circuit 603.

On the other hand, Sidiropoulos et al. discloses an identical phase comparator (see Fig. 7) with the phase comparator shown in Fig. 6 of the instant application. The phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle

imperfections and still providing an accurate phase lock (page 1688, left column, lines 3-5). Since the phase comparator of Sidiropoulos et al. and the phase comparator shown in Fig. 6 of the instant application have exactly the same structure and perform the same function (i.e., phase comparison between the delayed clock signal and the clock signal), it is clear that the phase comparator of Sidiropoulos et al. performs the same steps as recited in claim 28.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the phase comparator taught by Sidiropoulos et al. in place of the phase comparator of Tamura in view of Lai to detect a delay skew between the delayed clock signal and the clock signal, since the phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock.

Regarding claim **29**, Tamura teaches the claimed invention (see the rationale applied to claim 26 above), but fails to teach that the step of detecting the delay skew includes the steps of generating a first pulse, generating a second pulse, resetting a latch circuit using the first pulse, and setting the latch circuit using the second pulse, wherein all steps are performed by the phase comparator shown in Fig. 6 of the instant application. The step of generating a first pulse is performed by the first pulse generator 602 in Fig. 6. The step of generating a second pulse is performed by the second pulse generator 601 in Fig. 6. The step of resetting a latch circuit using the first pulse is achieved by sending the pulse 611 to the latch circuit 603. The step of setting the latch

circuit using the second pulse is achieved by sending the pulse 610 to the latch circuit 603.

On the other hand, Sidiropoulos et al. discloses an identical phase comparator (see Fig. 7) with the phase comparator shown in Fig. 6 of the instant application. The phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock (page 1688, left column, lines 3-5). Since the phase comparator of Sidiropoulos et al. and the phase comparator shown in Fig. 6 of the instant application have exactly the same structure and perform the same function (i.e., phase comparison between the delayed clock signal and the clock signal), it is clear that the phase comparator of Sidiropoulos et al. performs the same steps as recited in claim 29.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the phase comparator taught by Sidiropoulos et al. in place of the phase comparator of Tamura in view of Lai to detect a delay skew between the delayed clock signal and the clock signal, since the phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock.

Allowable Subject Matter

11. Claims 5-9, 12-15, 30 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all

of the limitations of the base claim and any intervening claims and rewritten to overcome the claim objections in Paragraph 3 of this Office Action.

12. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Claims 17-25 would be allowable if rewritten or amended to overcome the claim objections in Paragraph 3 of this Office action.

14. The following is a statement of reasons for the indication of allowable subject matter:

Claims 5-9 are allowable over the prior art of record because the prior art of record does not teach or suggest that the amplifier includes a current mirror load, a bias transistor, a first differential input transistor and a second differential input transistor.

Claims 12-15 are allowable over the prior art of record because the prior art of record does not teach or suggest that the charge pump circuitry includes a second current source receiving the first supply voltage, the second current source having a control electrode to receive the bias control signal, a second load transistor coupled to the first reference terminal, wherein the second load transistor responds to the first pump output; and a second input transistor coupled in series between the second

current source and the second load transistor, the second input transistor responsive to a second phase input to provide a charge pump output.

Claim 16 is allowable over the prior art of record because the prior art of record does not teach or suggest that the supply voltage is provided to the multiplexer circuit and the interpolation circuit.

Claims 17-25 are allowable over the prior art of record because the prior art of record does not teach or suggest the operational amplifier includes a bias transistor biased by a bias voltage, and a bias generator to provide the bias voltage, wherein the bias generator having a first input coupled to the control signal and a second input to receive the bias voltage.

Claims 30 and 31 are allowable over the prior art of record because the prior art of record does not teach or suggest that the step of tracking the voltage signal includes amplifying a voltage differential between the first input and the second input, biasing the current source with a bias signal, and generating the supply voltage at the output, wherein the supply voltage is proportional to the voltage differential.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dally et al. (US Patent 6,316,987) teaches a low-jitter variable delay timing circuit. Thoma et al. (US Patent 5,672,991) teaches a differential delay line circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chieh M Fan whose telephone number is (703) 305-0198. The examiner can normally be reached on Monday-Friday 8:00AM-5:30PM, Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (703) 305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.

Chieh Min Fan
Chieh M Fan
Examiner
Art Unit 2634

cmf
April 12, 2002

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PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RMBS.002	SERIAL NUMBER 09/303,669
	APPLICANT S. SIDIROPOULOS	
	FILING DATE MAY 3, 1999	GROUP ART UNIT 2734

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
cf	5,727,037	03/10/98	Maneatis	327	158	
cf	5,614,855	03/25/97	Lee et al	375	376	
cf	5,796,673	08/18/98	Foss et el.	365	233	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

cf	J. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," IEEE Journal of Solid-State Circuits, vol, 31, no. 11, pp. 1723-1732, (Nov. 1996)
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cf	M. M. Griffin et al., " A Process-Independent, 800-MB/s DRAM Byte-Wide Interface Featuring Command Interleaving and Concurrent Memory Operation", IEEE Journal of Solid-State Circuits, vol, 33, no. 11, pp. 1741-1751, (Nov. 1998)
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	FILING DATE MAY 3, 1999	GROUP ART UNIT 2734

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
CF	5,412,349	05/02/95	Young et al.	331	34	
CF	5,334,953	08/02/94	Mijuskovic	331	8	
CF	5,477,193	12/19/95	Burchfield	331	8	
CF	5,687,201	11/11/97	McClellan	375	376	
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EXAMINER Chuk Mui Fan	DATE CONSIDERED 4/11/02

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Notice of References Cited	Application/Control No. 09/303,669	Applicant(s)/Patent Under Reexamination SIDIROPOULOS, STEFANOS	
	Examiner Chieh M Fan	Art Unit 2634	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-6,247,138	06-2001	Tamura et al.	713/600
	C	US-5,672,991	09-1997	Thoma et al.	327/239
	D	US-5,339,009	08-1994	Lai	315/291
	E	US-			
	F	US-			
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	N					
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	P					
	Q					
	R					
	S					
	T					

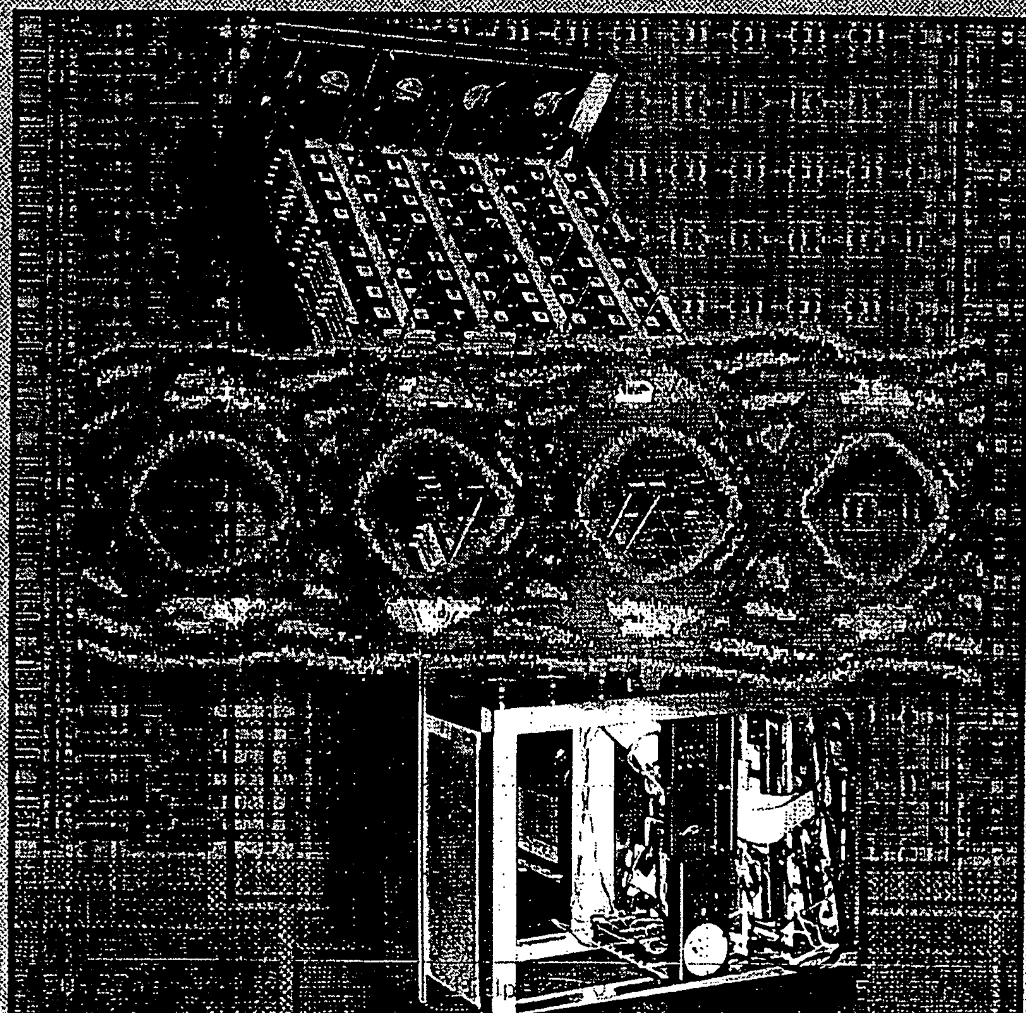
NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Dally et al., Digital Systems Engineering, cambridge, 1998, pp. 589-607.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

DIGITAL SYSTEMS ENGINEERING

WILLIAM J. DALLY   JOHN W. POULTON



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Author	Dally, William J.
Title	Digital systems engineering / William J. Dally, John W. Poulton.
Imprint	Cambridge, U.K. : New York, NY, USA : Cambridge University Press, 1998.
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12 TIMING CIRCUITS

This chapter presents circuit and design details for clocked circuits (latches and flip-flops) and clock-generating circuits (controlled delay lines and oscillators). We show how the basic circuit elements presented in Chapter 4 can be combined to produce robust timing and clocking elements to implement the timing and synchronization systems of Chapters 9 and 10.

in Figure 12-25(c). However, the outboard form has a potential charge-sharing hazard, as illustrated in the waveforms in Figure 12-25(b). Suppose that D is low as clk goes high and that X is high, driving the Q output low. After the master latch has become opaque, D makes a low-to-high transition, which turns on the NFET between X and the clk-NFET in the master latch. If the parasitic capacitance on this in-between node C_{mid} is large compared with the input capacitance C_{in} of the slave latch, then charge sharing can bring X's voltage down low enough to reach the switching threshold of the slave, corrupting the output data. If the clocked FETs are placed inboard, as in Figure 12-25(c), the flip-flop is immune to this problem; this arrangement is always preferred.

As we have discussed, latch failures from dynamic node decay, power supply noise, clock slope sensitivity, and charge sharing are especially problematic for dynamic latches and flip-flops. This perhaps explains why dynamic storage, once popular in MOS design, has largely fallen out of favor. Dynamic circuits offers significant advantages for performance-driven designs, however, and should not be rejected out of hand without first considering various ways of coping with their infirmities.

12.2 DELAY LINE CIRCUITS

The clock-generation circuits we will discuss in the remainder of this chapter and have discussed in Chapter 11 all require generation of adjustable, low-jitter delayed clocks and often groups of equally spaced delayed clocks. Adjustment is needed so that delay elements can be placed inside control loops that stabilize delays (or edge placement, or phase) by comparing a delayed clock against a reference. Generally it is desirable to have a wide adjustment range to accommodate, for example, a wide range of clock frequencies. All practical delay elements are susceptible to noise injection from power supplies, both directly from supply terminals to signal outputs and indirectly through delay-control inputs to signal outputs. Both direct noise and delay modulation are sources of jitter in delay elements. In this section we will explore circuit techniques for constructing delay elements that provide widely adjustable clock edge placement, introduce as little jitter as possible, and reject noise from power supplies.

12.2.1 Inverter Delay Lines

A CMOS inverter can be used as a simple delay element, and a delay line can be built by cascading a number of inverters. An adjustable delay line could be constructed as shown in Figure 12-26.

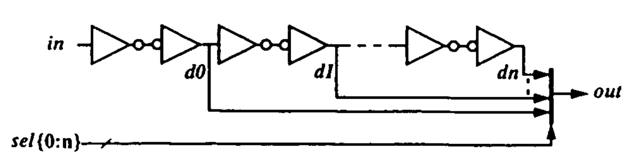


FIGURE 12-26 Inverter Delay Line

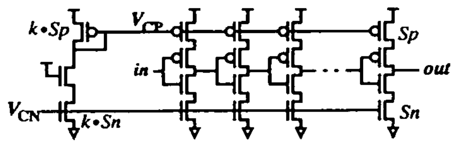


FIGURE 12-27 Current-Starved Inverter Delay Line

Here *pairs* of inverters are used so that all of the delayed versions of in have the same polarity. A multiplexer selects one of the delayed signals for output and sets the overall delay. There are several difficulties with this implementation.

1. Large delay range and fine-grain adjustment are mutually incompatible goals; if the difference in delay between two taps on this delay line is small, then many stages will be needed to realize a long overall delay, and jitter introduced at each stage will increase the jitter at the output as the square root of the number of stages.
2. The minimum delay adjustment step that is possible in a given technology, about two inverter delays, is often too coarse for high-precision, low-jitter applications. This problem can be solved with a more complex design in which inverter pairs with slightly different delays are used for vernier adjustment of the overall delay.
3. The digital delay adjustment of the delay line favors a digital control system to set the delay; as we will see, analog control systems are often more compact, power efficient, and accurate than their digital counterparts.

For all of these reasons it is desirable to find a delay element that has an analog control input.

The fundamental circuit elements that generate delay in an inverter delay line are FET current sources charging FET gate capacitances. Because FETs are voltage-controlled current sources, the most obvious way to add a voltage-mode control input is to add current control transistors in series with the switching transistors in the inverters. The current-starved inverter delay element we introduced in Figure 4-70 is used to form a delay line in Figure 12-27.

Another type of voltage-controlled inverter delay line is shown in Figure 12-28. Instead of controlling the charging current, this approach controls the capacitive load or, more precisely, the fraction of each 1-to-0 and 0-to-1 transition during which each inverter must charge its load capacitor. On a 0-to-1 transition at a delay stage, charging current flows into the load capacitor until the voltage on the capacitor reaches $V_{CN} - V_{TN}$, whereas on a 1-to-0 transition, the inverter must supply discharge current when the inverter output falls below this value. The load

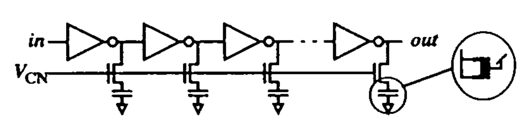


FIGURE 12-28 Capacitor-Loaded Inverter Delay Line

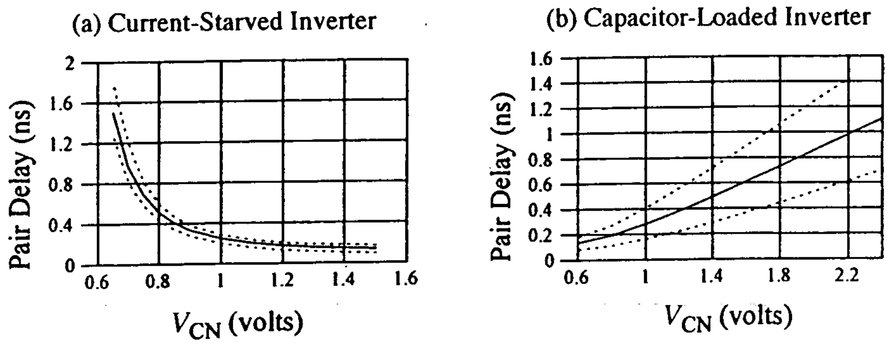


FIGURE 12-29 Delay Adjustment Range for Example Delay Elements

capacitors in this type of delay line are usually MOS capacitors. One possible implementation is shown in the inset of Figure 12-28, an NMOS capacitor with its gate connected to V_{DD} to ensure that its channel is biased well above V_{TN} (see Section 4.2.1.1). The source–drain junctions add some additional useful capacitance.

12.2.1.1 Delay Adjustment Range

Figure 12-29 shows the delay adjustment range from simulation of examples of the current-starved inverter delay line (a) and the capacitor-loaded delay line (b). Devices in the current-starved delay line are sized at $Sp = 2 \cdot Sn = 5.6\ \mu m/0.35\ \mu m$, $k = 10$ (S is the shape factor W/L for a device, k is the ratio used to size the current mirror that generates V_{CP} from V_{CN}). Switching FETs are drawn the same size as the current sources. The capacitor-loaded line uses devices of the same size and an NMOS capacitor drawn $28\ \mu m/2.8\ \mu m$. Delay for a pair of stages is shown, in order to sum the (typically different) rise and fall delays.

The solid lines in each graph represent simulated pair delay with the nominal FET parameters, $V_{DD} = 2.5$ V, and $T = 85°C$. Adjustment range is about 11:1 for the current-starved inverter delay element. Delays even larger than those plotted are possible, but the delay time's sensitivity to control voltage becomes so large that it becomes difficult to control jitter adequately. The capacitor-loaded delay element example gives about an 8:1 adjustment range; again, the delay range could be made larger but at the expense of an unreasonably large loading capacitor.

Although these delay ranges are obtainable for a particular set of FET models, power supply voltage, and temperature, we must usually design for worst-case behavior. The dotted curves represent our simulation of these conditions. The maximum delay is obtained under conditions of slow FET models, low supply voltage (2.25 V), and high temperature ($T = 110°C$). Minimum delay is found for conditions of fast FET models, high supply voltage (2.75 V), and low temperature ($T = 25°C$). The actual delay range we can count on lies between the largest delay we can get under best-case conditions and the smallest delay under worst-case conditions (about 7:1 for the current-starved inverter and only about 3.8:1 for the capacitor-loaded inverter).

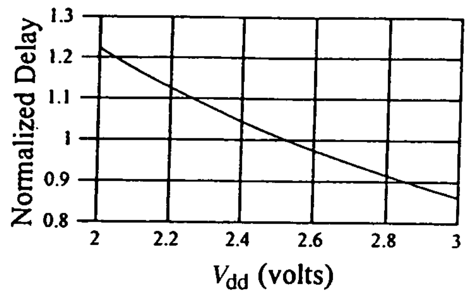


FIGURE 12-30 Power Supply Sensitivity of CMOS Inverter

12.2.1.2 Power-Supply Rejection in Inverter Delay Elements

Current-starved, capacitor-loaded, and simple inverter delay elements were used extensively in early designs (1980s) for on-chip phase-locked and delay-locked loops and are described in several of the references. These approaches have fallen out of favor in more recent designs because high-performance delay elements require much better power supply noise rejection than can be obtained in CMOS inverters.

To examine the inverter delay power supply sensitivity, we simulate a string of identical inverters and measure the delay through a pair of them. Figure 12-30 plots normalized inverter pair delay versus power supply voltage ($Sp = 2 \cdot Sn$, as above).

The graph indicates that the fractional variation in delay is about the same as the fractional variation in power supply voltage; a CMOS inverter has rather poor power supply rejection The slope of the curve can be understood from the τ-model we developed in Chapter 4. Equation (4-24) predicts that the delay per stage in an inverter chain should be

$$\tau_{\text{Delay}} \propto \frac{V_{\text{DD}}}{I_{\text{DSS}}} \propto \frac{V_{\text{DD}}}{(V_{\text{DD}} - V_{\text{T}})^2} \tag{12-1}$$

if we assume that the driving transistor is in saturation during most of the time an inverter is charging its output load. Roughly, delay should go as $1/V_{\text{DD}}$.

Supply sensitivity for a current-starved inverter delay element is shown in Figure 12-31. In this delay element, charging current is set by the current-source

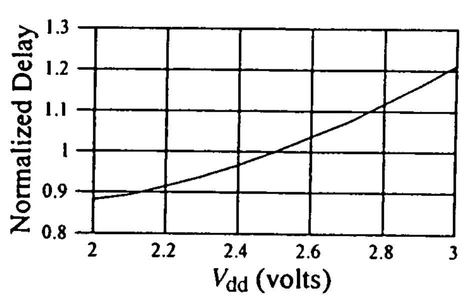


FIGURE 12-31 Supply Sensitivity for Current-Starved Inverter

FETs; consequently, our simple τ-model predicts that the delay should vary roughly as V_{DD}.

Though the slope of the power supply sensitivity curve for the current-starved inverter is opposite that of the simple inverter, the magnitude of the sensitivity is just as bad.

For purposes of this discussion, we define the supply sensitivity S_V as the fractional change in delay divided by the fractional change in supply voltage. The S_V is about 0.9 for the inverter, about 1.5 for the current-starved inverter delay element at the low end of the V_c range, and about 2.0 for the capacitor-loaded delay element. Noise on the power rails of an inverter delay line of any of the types we have described will produce large amounts of timing jitter.

12.2.1.3 Inverters with Regulated Supply Voltage

Because the main infirmity of inverter-based delay stages is power-supply sensitivity, we could attempt to improve their performance by stabilizing the power supply in some way. The simplest technique is to add a low-pass filter between the supply source and a "clean" supply dedicated to the delay elements, as shown in Figure 12-32(a). Only the high-frequency part of the supply noise is removed, but if the cutoff frequency of the filter is well within the bandwidth of the delay control loop, this may be a winning strategy. In Figure 12-32(b), an active series regulator cleans up the supply. The reference voltage V_{ref} could be generated on-chip (e.g., in a band-gap reference).

It is even possible to make a virtue of the inverter's large supply voltage sensitivity. One of the references [vonKaen96] uses the supply terminal as the delay adjustment control input; the implementation in this reference is much like Figure 12-32(b), using V_{ref} as the delay control input; the control loop filter is also incorporated into the regulator.

12.2.2 Differential Delay Elements

Delay in a CMOS stage such as an inverter is proportional to the charge that must be moved to switch the next stage and is inversely proportional to the current available to do the charging. In the current-starved delay line we made the charging current nearly independent of supply voltage. However, the charge movement needed to switch the next stage is proportional to the supply voltage (it appears explicitly in the switching threshold for the inverter, Eq. (4-18)).

Differential structures (Section 4.3.6) amplify the difference between two voltages rather than the difference between a voltage and built-in reference that

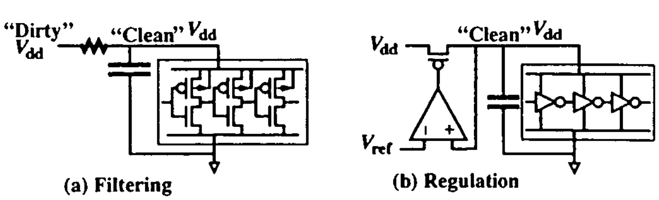


FIGURE 12-32 Supply Filtering for Delay Elements

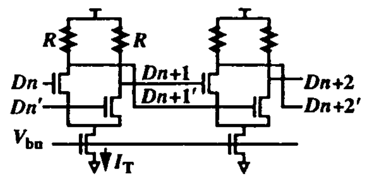


FIGURE 12-33 Differential Delay Elements

depends on the power supply voltage, and consequently a differential amplifier used as a delay element inherently has better supply-noise rejection than an inverter. An example of a delay line composed of differential amplifiers is sketched in Figure 12-33.

Each signal pair in the delay line swings between V_{DD} and $V_{LO} = I_T R$, where the differential tail current I_T is set by the bias voltage V_{bn}. In Section 4.3.6 we showed that the differential amplifier has a low-pass response given by Eq. (4-61). The stage delay is proportional to the load resistance in the stage, R, and thus we can vary the delay in a differential delay line by varying R. For ideal elements in the differential pair and for resistive loads, changes in the power supply voltage change only the common-mode voltage on the D, D' pairs; consequently, under these assumptions power supply noise will produce no jitter in stage delay. It is possible in practice to approach this ideal fairly closely. It remains to show how to construct loads that are adjustable (to control the delay) and as nearly resistive as possible (to reject power supply noise).

12.2.2.1 Adjustable PFET Resistor

In Section 4.3.6.5 we discussed the two-element FET resistor (Figure 4-61b) [BabaTeme84, MoonZagh90, GabaKnau92]. This arrangement combines the diode-like drain characteristics of a FET whose $V_{GS} = V_{DS}$ with the triode-like characteristic of a biased FET (V_{GS} = constant). The opposite curvatures of the two characteristics combine to give an S-shaped, nearly resistive one. Figure 12-34

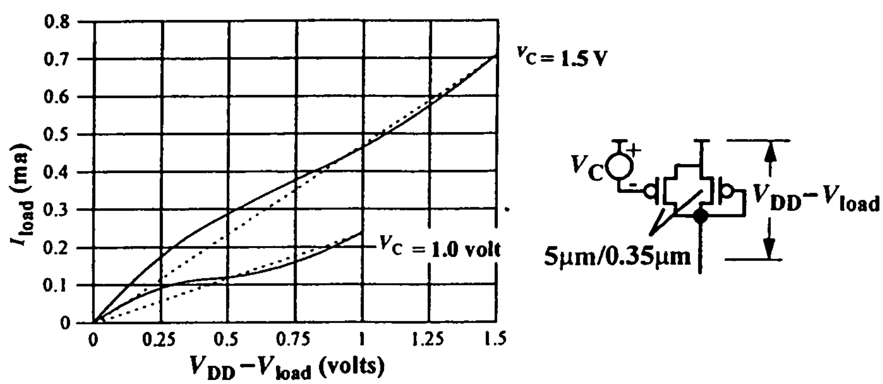


FIGURE 12-34 Voltage-Controlled Two-Element PFET "Resistor"

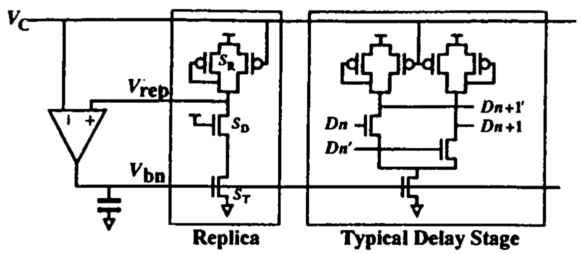


FIGURE 12-35 Replica-Biased Differential Delay Line Circuitry

shows the results of a SPICE simulation in which the "triode" V_{GS} is set by a control voltage V_C; the currents for two different control voltages are shown.

If the voltage swing across the load is limited between 0 and V_C, then the characteristic of this load is approximately resistive, and the resistance is set by the control voltage, V_C. The load is a transconductance controlled by V_C, and we can find its small-signal value by computing dI/dV at a convenient point, namely where $V_{load} = V_C$. Both FETs are in saturation, and thus if we ignore channel-length modulation, the current through each of the two FETs at this point is $\beta_P(V_C - V_{TP})^2$, and the transconductance is approximately

$$g_m = \frac{\delta I}{\delta V_C} = 2\beta_P(V_C - V_{TP}) \tag{12-2}$$

The low end of the signal swing in the differential stage can be set to any desired value by adjusting the tail current, I_T, appropriately. In a differential delay line, V_{LO} can be held at V_C by controlling I_T with a replica bias circuit like that of Figure 4-63(b).

12.2.2.2 Replica-Biased Delay Line

The circuitry for a replica-biased differential delay line is shown in Figure 12-35. Delay is set by the control input, V_C, which varies the effective resistance of the loads in the delay elements and thus varies the delay. The replica bias feedback adjusts the tail current by means of the bias voltage, V_{bn}, so that the "low" output of the replica, V_{rep}, tracks V_C. The replica is a duplicate of the "on" side of a typical delay element. This arrangement keeps the signal swing in the delay elements within the most linear part of the two-element resistor's characteristic.

12.2.2.3 Adjustment Range for Replica-Bias Delay Lines

Delay in a replica-biased delay element is proportional to C_{load}/g_{mload}, and from Eq. (12-2)

$$T_D \propto \frac{C_{load}}{V_C - V_{TP}} \tag{12-3}$$

where C_{load} is the sum of the next-stage gate capacitance and parasitic wiring and drain capacitances. Figure 12-36 is a plot of single-stage delay versus control

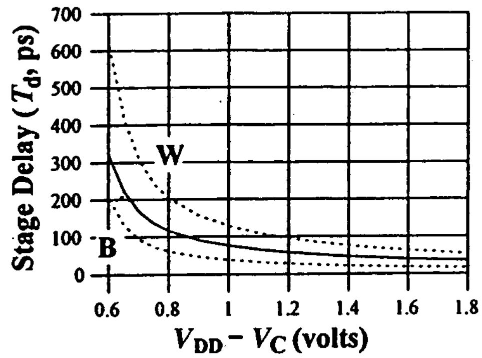


FIGURE 12-36 Delay Adjustment Range for Replica-Biased Delay Element

voltage for an example replica-biased delay line (with replica stage shape factors $S_R = 5\,\mu m/0.35\,\mu m$, $S_D = 10\,\mu m/0.35\,\mu m$, $S_T = 20\,\mu m/0.35\,\mu m$). The dotted lines show the delay at the same extrema of fabrication, V_{DD}, and temperature used in Figure 12-29. The shape of the curve is consistent with Eq. (12-3).

For control voltages less than 100 mV or so above V_{TP}, signal swings become very small and delay gain ($\delta T_d/\delta V_C$) so large that noise on V_C, amplified by this gain, introduces unacceptable jitter. The practical range of adjustment for this stage is about 10:1 for any of the three simulations in the figure; taken across best- and worst-case operating conditions, adjustment range is about 4:1.

It should be noted that the adjustment range of a delay line can be greatly extended by having a two-tier adjustment scheme. In such a scheme, fine adjustment is accomplished by varying the control voltage, as we have discussed, but coarse adjustment is added, for example, by digitally selecting the number of delay stages in the delay line. Coarse adjustment would most likely be made only at system initialization.

12.2.2.4 Static Supply Sensitivity for the Replica-Biased Delay Stage

Figure 12-37 is a plot of stage delay versus V_C for the example replica-biased delay stage and supply voltages of 2.25 and 2.75 V (±10% of nominal 2.5 V).

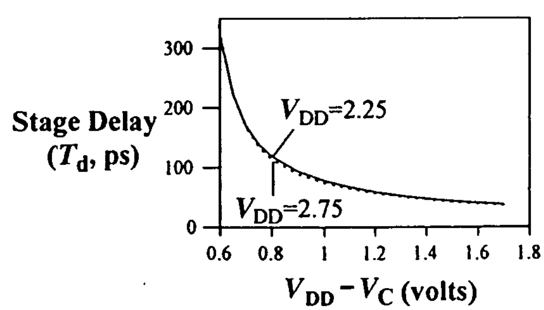


FIGURE 12-37 Static Supply Sensitivity for Replica-Biased Delay Element

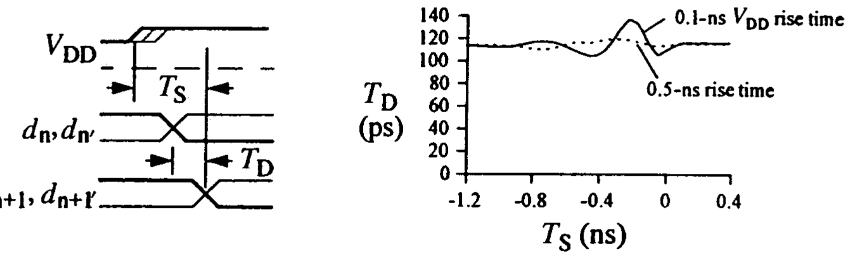


FIGURE 12-38 Dynamic Supply Sensitivity Simulation

Worst-case S_V is about 0.2 for this example, about an eightfold improvement over the current-starved inverter.[1]

12.2.2.5 Dynamic Supply Sensitivity

So far we have described the static supply sensitivity of various delay elements. Power supply noise may have significant high-frequency components, and these will introduce jitter that is worse than would be predicted from an estimate based only on static supply sensitivity. High-frequency supply noise will introduce jitter not only directly, by modulating the drain currents and switching thresholds of various devices, but indirectly through the device and wiring parasitic coupling capacitances. In a replica-biased differential delay line, supply noise at frequencies above the cutoff of the bias control loop cannot be compensated by the loop, and consequently the "resistors" will be moved away from their optimal operating range in a transient way.

Dynamic supply sensitivity is difficult to simulate because it is not easy to predict the nature of the noise on the supply rail. We can perform a far from perfect, but useful, evaluation of a delay element's resistance to transients on the supply voltage by running a simulation outlined in Figure 12-38. Using the example replica-biased delay line, with $V_{DD} - V_C$ fixed, we introduce a 0.1-ns 0.25-V step in V_{DD} at time T_S measured with respect to a signal transition within the delay line. We then determine the delay through an element as a function of T_S, marching the V_{DD} edge past the signal transition edge to find the worst-case interaction. As shown in the graph in the figure, the transient disturbance in stage delay is about 20%, which is much larger than the 2% static sensitivity. However, with a 0.5-ns V_{DD} edge, delay varies by only about 5%, as shown in the dashed line in the plot.

The results of this simulation can be understood with the model shown in Figure 12-39. R_L and R_H are the resistances of the inverting and noninverting

[1] Significantly better supply rejection can be obtained in practice. Our level-3 PFET model does not adequately capture the behavior of devices in real submicron processes in which PFETs have significantly worse channel-length modulation than we have shown and an extended transition region. Although these characteristics make PFETs rather poor switches, they are excellent resistors, much better than indicated in Figure 12-34. Better device modeling and more careful attention to circuit optimization will yield better results than in our example delay line. Some of the designs in the references claim supply sensitivities for replica-biased delay elements as low as 0.012.

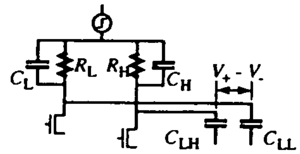


FIGURE 12-39 AC Equivalent Circuit for Supply Noise Injection

output loads in a differential stage, C_L and C_H are the capacitances across the loads, and C_{LH} and C_{LL} are the input capacitances of the next stage. The capacitances across the load devices are mostly due to the sum of the overlap capacitance, C_{GSO}, of the diode-connected PFET in the load, its channel capacitance, and C_{GDO} of the V_C-controlled PFET (the controlled PFET's gate is connected via a low AC impedance to V_{DD}). The input capacitances are the sum of the channel capacitances and (Miller-effect-enhanced) overlap capacitances. These capacitances vary with the operating point of the load device (Section 4.2.1), and their nonlinearities translate an AC voltage on V_{DD} to a differential voltage across the next stage input.

Because supply noise injection is high-passed by the load devices in a differential stage, removing the high-frequency part of the supply noise above the cutoff of the loads will mitigate the effect. Methods for dealing with the problem include careful supply network design, bypass capacitance local to the delay elements, and perhaps addition of some intentional series resistance in the supply network between noise generators and delay elements.

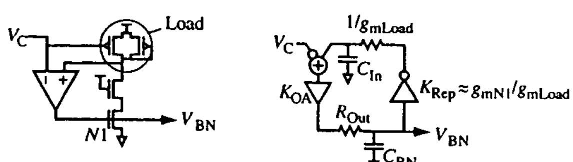
12.2.3 Circuit and Layout Details

This section discusses some of the details for designing delay lines and VCOs.

12.2.3.1 Replica Control Loop Stability

The replica bias circuitry is a control system that must be guaranteed stable for correct operation. A replica bias generator is shown in Figure 12-40(a) and an approximate AC equivalent circuit is shown in (b).

Typical (simple) CMOS operational amplifiers have gains of 50–100, whereas the gain of the replica stage is roughly $g_{mN}/g_{mLOAD} \approx 5$–$10$, and thus typical loop gain is about 1,000. Poles are introduced into the transfer function at the outputs of the two gain stages. One is formed by the output resistance of the operational amplifiers and the capacitance of the parallel collection of tail transistors, and another is formed by the conductance of the symmetric load and the input capacitance of the operational amplifier.



(a) Replica bias circuit (b) Approximate AC equivalent circuit

FIGURE 12-40 Replica Bias Control Loop

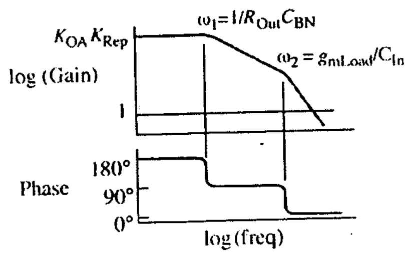


FIGURE 12-41 Bode Plot of Replica-Bias Control Loop

A Bode plot for the open-loop gain of the controller will look like Figure 12-41. If the poles are very close together, the 12 dB/octave rolloff causes the phase to reach 0°, at a frequency at which the gain is greater than unity; under these conditions, the loop will be unstable. Stability is usually ensured by moving the pole associated with the operational amplifier's output downward in frequency until there is a "safe" phase margin at unity gain. (A typical rule of thumb requires >35° or so of phase margin.) Note that loop instability will be worst at high loop gain and low ω_2, both of which conditions occur at the smallest value of $V_{DD} - V_C$ (smallest load conductance) and under best-case fabrication, high supply voltage, and low temperature.

The frequency of the operational amplifier's output pole can be reduced by increasing the output resistance of the amplifier (which generally reduces its power consumption) or by increasing the capacitance on V_{BN}. Additional capacitance lowers the AC impedance between V_{BN} and GND and helps prevent noise injection into the V_{BN} node. The lower limit on the bandwidth of the replica-bias control loop is established by the need to track changes in the timing control voltage, V_C, and thus the replica-bias loop bandwidth should at least be greater than the bandwidth of the timing control loop. Note that there may be other poles and zeros in the loop circuitry that affect loop stability; simulation with an accurate model of circuit parasitics extracted from the layout is required in this part of the design of a timing loop.

Any of a variety of operational amplifiers designs will work well in this application. The authors have successfully used simple self-biased amplifiers (like the Chappel amplifier of Section 11.3.1.2). A particularly clever approach [ManeHoro93] provides the operational amplifier's tail current bias from its own output. The scheme is outlined in Figure 12-42.

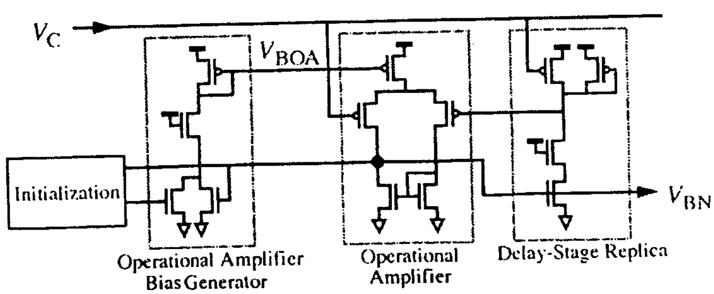


FIGURE 12-42 Self-Biased Operational Amplifier for Replica Bias Generator

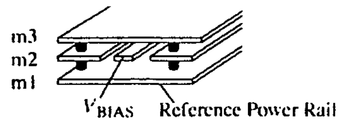


FIGURE 12-43 Electrostatic Shielding for a Critical Bias

The operational amplifier is a PFET differential pair whose tail current is set by the bias voltage V_{BOA}. This current is, in turn, set by the replica bias voltage, V_{BN}, which establishes the current in the operational amplifier's bias generator. This arrangement allows the operational amplifier's bias to be independent of power supply fluctuations. However, there are two stable operating points for the operational amplifier bias current, and one of them is at zero current. To avoid this operating condition, a bias initialization circuit is required that, upon power-up, ensures that some current is flowing in the operational amplifier's tail transistor and that V_{BN} is high enough to sustain operation after initialization.

12.2.3.2 Power Routing and Bypassing

Generating accurate delays with controlled delay elements requires distributing precise bias voltages from a central generator to an array of delay elements. Noise on the distribution networks for these biases introduces jitter in the intended timing relationships; voltage drops introduce systematic errors.

The two lines of defense against noise injection are isolation and bypassing. Isolation attempts to reduce noise injected directly into a bias line by increasing the impedance of the coupling mechanism, usually capacitive. The layout of delay circuits should, for example, avoid passing signal wires near bias wires. Where multiple levels of metal interconnect are available, it may be possible to construct partial or full electrostatic shields around bias lines, as shown in Figure 12-43.

Bypassing reduces noise by placing a low impedance between the bias line and its reference power supply. In the delay circuits we have described in this chapter, capacitance is often required to establish a stabilizing pole in a control loop transfer function. By distributing this capacitance across the area of a delay circuit and connecting it robustly to the appropriate reference power supply, the often large area required for the capacitor does double duty as control loop and bypass capacitor.

Bypassing a critical bias voltage to its reference supply also has the benefit that noise injected into the power supply will have less effect on the bias condition we are trying to enforce. If the reference supply is noisy, but the bias is bypassed to it via a low AC impedance, then the bias voltage will tend to move with the supply in such a way that biased devices see a fixed gate–source voltage. Noise on the supply itself should be reduced as far as possible by filtering and bypassing.

The metal-oxide semiconductor capacitors are FETs with only one source–drain terminal. The channel length associated with these devices introduces a series "resistance" that sets a lower limit on the high-frequency impedance. Metal-oxide semiconductor capacitors should therefore be drawn as wide as practicable and not too long. Significant AC currents flow through loop and bypass capacitors,

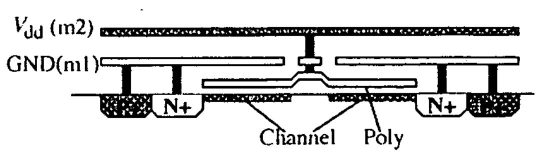


FIGURE 12-44 Cross Section of Power Bus Pair with Bypass Capacitor

and therefore they should have large-area well or substrate contacts adjacent to or abutting their source–drain terminals. A layout that efficiently combines a bypass capacitor and a power bus pair is shown in Figure 12-44; additional useful capacitance is obtained from the overlap of the metal and polysilicon wiring layers in this layout. A PMOS capacitor provides the additional well–substrate capacitance at the cost of a second P+ guard ring.

Voltage drop in the power rails is also a serious concern, because a difference in supply voltage between bias generator and biased device also changes V_{GS}. This is particularly true in circuits that consume static current. Voltage drop induced by these currents on the supply wiring series resistance introduces a systematic error in bias conditions and therefore timing. The best line of defense against this problem is robust power distribution wiring.

These points and recommendations are summarized in Figure 12-45.

1. Design robust power wiring to reduce resistance and minimize bias shifts.
2. Use metal-only wiring for bias voltages; series resistance in bias distribution may introduce additional unwanted poles in control functions.
3. Distribute loop control capacitors and tie them robustly to respective reference power supplies; capacitors do double duty as bypass elements.
4. Avoid coupling between bias and signal wiring; electrostatic shielding may be helpful.
5. Use filters and bypass power supplies to reduce noise.

12.2.3.3 Matching and Balancing

The offset voltage induced by transistor mismatches in differential timing circuits leads to systematic timing errors; therefore, care should be taken to use layout styles that promote good matching, as outlined in Chapter 11. Layouts for delay

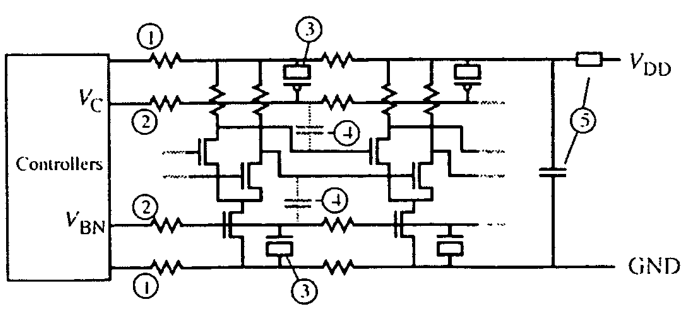


FIGURE 12-45 Layout, Wiring, and Bypassing Concerns for Delay Elements

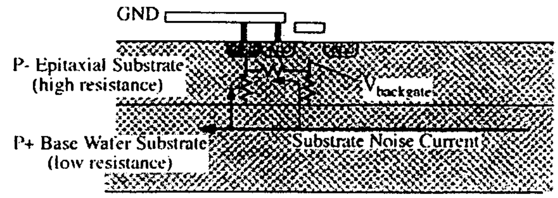


FIGURE 12-46 Substrate Noise Injection

lines that are intended to generate a set of equally spaced clocks also require very careful attention to parasitic capacitances in signal wiring. These capacitances should be balanced for each differential signal pair and be equal for all pairs. If buffering is needed for some, but not all, delay line outputs, the unbuffered delay stages require a "dummy" buffer to keep capacitive loads equal on all stages. The source-coupled node in differential timing stages also deserves careful attention in layout. Capacitance on this node shunts the current source, and thus the power supply isolation afforded by the current source's high impedance is rendered less effective at high frequency.

12.2.3.4 Substrate Noise

In addition to the power supply and bias rails, differential delay elements also share a substrate terminal. Modern "epi" CMOS processes feature a thin, relatively high-resistance P-type substrate (P−) grown epitaxially on top of a relatively low-resistance P-type base wafer material (P+), as shown in Figure 12-46. Source and drain terminals for NFETs and PFET N-wells are diffused into the epitaxial P− layer. The epi arrangement is intended to reduce the possibility of latchup by diminishing the effectiveness of lateral parasitic bipolar devices, thus allowing PFETs and NFETs to be spaced closer together to achieve higher circuit density.

The substrate terminal of an NFET is near ground potential, and an ohmic P+ diffusion into the P− epi substrate is provided so that metal ground conductors can be connected periodically to the substrate to help enforce this condition. The underlying, low-resistance P+ material is connected vertically to the ground system only through the P− substrate and unfortunately tends to acquire a voltage different from ground potential because of currents injected from many noise sources distributed over a chip. Because it has low resistance, these currents "tunnel" along under the high-resistance P− for long distances. Locally, there will be voltage difference between the underlying P+ material and the P− substrate. This voltage, measured under the gate of a typical NFET, is divided by the resistance of the epi layer to the nearest P+ substrate contact. If the substrate noise is large, the "back-gate" voltages for a collection of nearby NFETs may differ, and in a delay line this variation perturbs biasing conditions and introduces jitter. Even large, robust P+ ohmic contacts will not be particularly effective in shunting noise currents away from NFETs and in fact are likely to be detrimental.

Because PFETs are situated in an N-well, they are not seriously affected by these long-range substrate disturbances.

[VergSchm95] provides a good introduction to the problem of substrate noise. A recommendation for mixed-signal CMOS chips developed in this reference

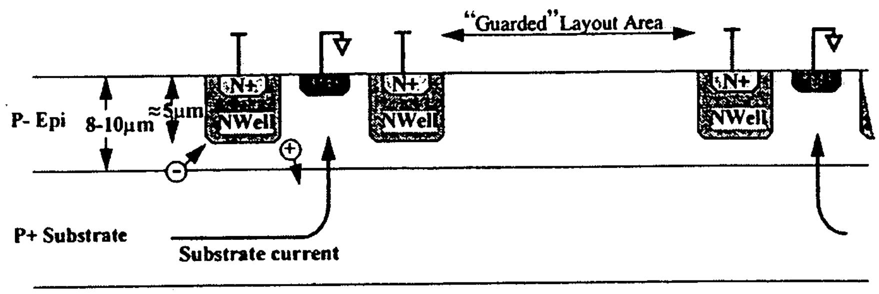


FIGURE 12-47 N-Well Noise Isolation Structure

may be useful in the context of precision delay lines. An N-well structure is used to protect analog circuits from free carriers and noise transmitted through the P+ substrate, as shown in Figure 12-47.

N+ and P+ regions are diffused only a micron or so into the epitaxial substrate, but N-wells are driven 4–5 μm into the epi, itself only 8–10 μm thick. N-wells biased at V_{DD} establish large depletion regions that trap free electrons and force free holes into the underlying P+ substrate, thereby forming a barrier against free carriers. The grounded P+ substrate contacts are "protected" by this arrangement and substrate currents terminate on these contacts. The epi substrate in the region between these guard structures should have nearly constant potential and is therefore "safe" for building well-matched NFETs; no P+ substrate contacts are allowed in the "guarded" region, for these contacts would shift the substrate potential.

12.2.4 Other Differential Timing Components

12.2.4.1 Small-Swing to Full-Swing Buffers

The signals within a differential delay line have small swings referenced to one of the supply rails. In many applications a buffer is needed to convert small-swing to full-swing signals. Such a buffer should isolate the small-swing delay-element signals from noise on the full-swing outputs, and the delay through the buffer should be as insensitive as possible to supply voltage variation. Various types of gate-isolated differential buffers can be constructed to meet both these requirements.

A simple buffer is shown in Figure 12-48. This buffer consists of two stages. The first converts the small-swing differential voltage input to a differential pair of currents that produce bias voltages $V1, V2$ in the NFET's sized Sn. These biases generate currents scaled by k in the second stage, whose current-mirror load converts the differential currents into a full-swing output. The factor k can be larger than 1 so that a large load can be driven on B while keeping the input capacitance on D, D' small. If B' is needed, a second copy of the second stage can be added, with its current mirror reversed. Because the current in the second stage is set by the voltage swing at the inputs, it might appear that the delay through this buffer has first-order supply sensitivity similar to the current-

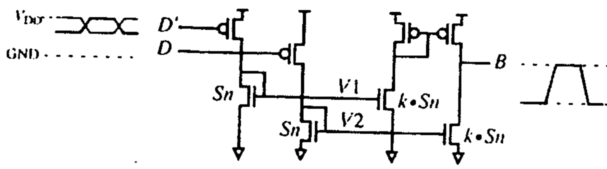


FIGURE 12-48 Differential Output Buffer

starved inverter (proportional to V_{DD}). However, the channel-length modulation in the PFETs in the circuit compensates by supplying more current at higher supply voltages; therefore, the buffer's delay is fairly insensitive to supply voltage variation.

A buffer developed in [Maneatis96] takes advantage of the replica-bias conditions established for the delay elements to construct a buffer that also uses the replica-bias tail current, thereby tracking the voltage swings within the delay elements. This approach, sketched in Figure 12-49, also uses a current-mirror load to convert a small-swing signal to a full-swing one. As in Figure 12-48, if B' is needed, a second copy of the output stage can be added with the current mirror reversed.

12.2.4.2 Interpolators

It is often useful to interpolate between two fixed delay values to generate a third. In a replica-biased delay line, an auxiliary circuit that uses the same replica-bias conditions as the delay elements can perform interpolation, as shown in Figure 12-50.

The interpolator is drawn as nearly identically to the typical delay stage as possible but has two current-tail transistors and two differential pairs. The two current-tail transistors have shape factors that are scaled down from the tail transistor in the typical delay stage, but the shape factors add up so that the total current through the load is the same as in the typical delay stage. If the inputs Da,Da' and Db,Db' are from a delay stage spaced n stages apart in a delay line, then, assuming $k1+k2=1$ and ignoring differences in parasitic capacitances between the interpolator and a typical delay stage, the output of the interpolator introduces a fixed delay of one delay stage (Td) plus a delay that is adjustable between 0 and $n \cdot Td$ by varying $k2$ (while keeping $k1+k2=1$). The example in Figure 12-50 shows a replica-biased interpolator, but any differential stage will perform interpolation weighted by the tail currents.

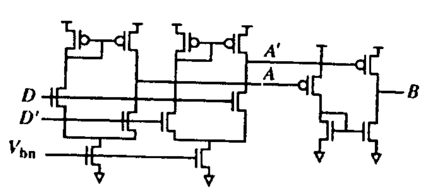


FIGURE 12-49 Replica-Biased Output Buffer

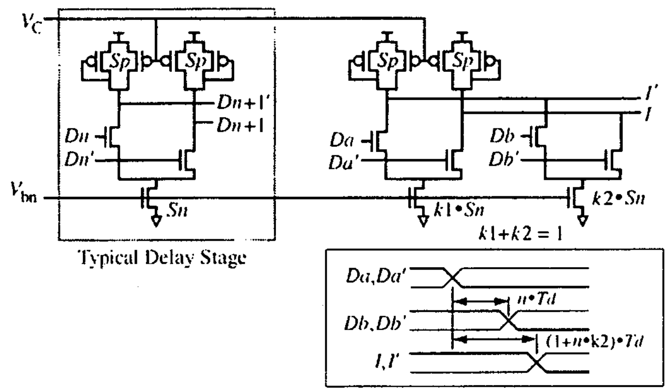
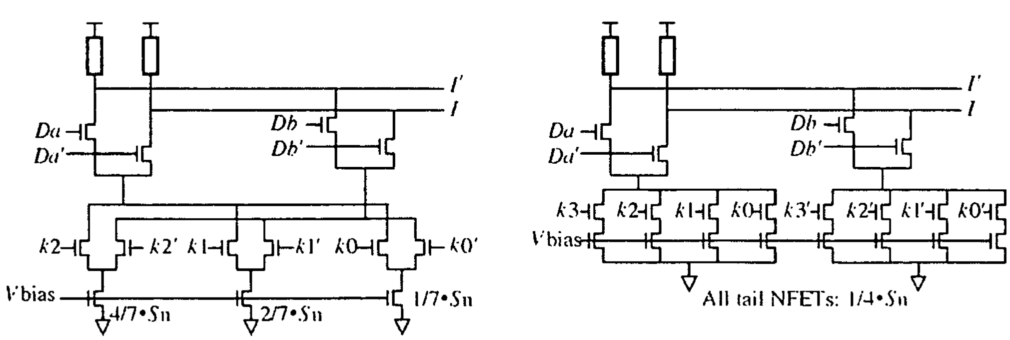


FIGURE 12-50 Replica Biased Interpolator

It is usually desirable to control the interpolation value. Two methods for digitally setting the interpolation factor are shown in Figure 12-51.

In Figure 12-51(a), the current delivered to the two differential pairs is determined by a binary-weighted set of three current tails. When $k\{2:0\} = 111$, all of the current is delivered to the left-hand differential pair, and when $= 000$ all is delivered to the right-hand pair. Other codes on k interpolate I,I' between the Da and Db inputs.

Binary weighting may present difficulties for some applications. First, it may be difficult to construct current tail transistors that are $1/(n-1)$ sized; in fact, the most accurate way to perform this sizing is to make full-sized current tails $(1 \cdot Sn)$ by paralleling $(n-1)$ identical devices. Second, the transition between certain codes (e.g., $011 \rightarrow 100$) may introduce glitches in the output. To avoid these problems, a thermometer-coded version of the adjustment variable k can be used to switch equally weighted current tails. A possible implementation for a 2-bit k is shown in Figure 12-51(b). This version uses redundant copies of the current tail transistor to establish the tail current; it is convenient for layout but may introduce some common-mode noise into the output owing to charge injection at the nodes between tail transistors and switching transistors. The two



(a) Binary-Weighted Current Sources (b) Equally Weighted Current Sources

FIGURE 12-51 Digitally Adjustable Interpolators

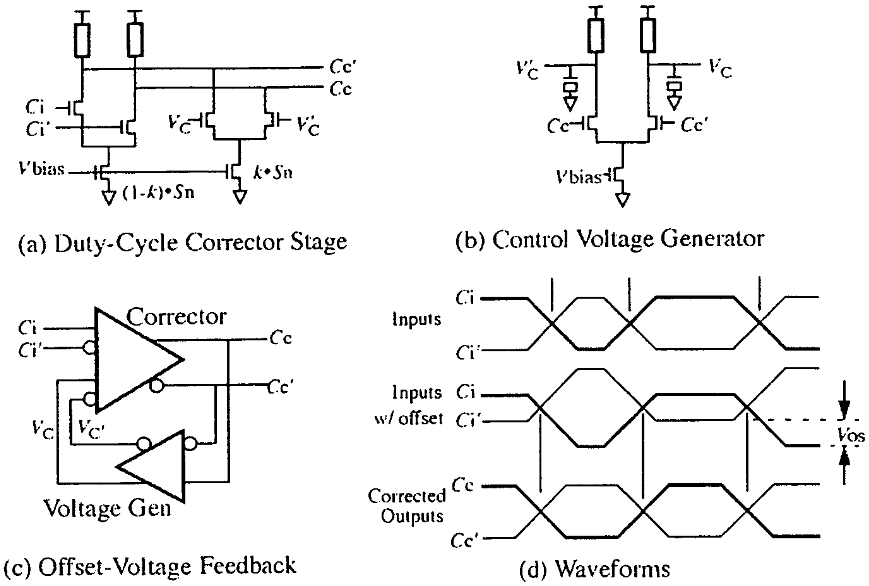


FIGURE 12-52 Duty Cycle Corrector

implementations are, of course, binary-weighted and monotonic digital-to-analog converters.

12.2.4.3 Duty-Cycle Correctors

For applications in which the timing of both edges of the clock is critical, the duty cycle of the signals within a delay line must be held at 50%. Active control of the duty cycle may be needed to compensate for variations in switching thresholds and other asymmetries in a delay structure and for voltage offsets in a reference clock, perhaps generated off-chip. A variation on the theme of the interpolator can be used to servo the duty factor of a differential clock toward 50%. A circuit for this function is outlined in Figure 12-52.

In Figure 12-52(a), a differential stage takes as input a signal pair Ci,Ci' whose duty factor is to be adjusted and outputs a corrected signal pair Cc,Cc'. Tail current is split between two differential pairs, one of which gets the signal pair while the other gets a differential control voltage V_c,$V_{c'}$. Under the usual simplifying assumptions for differential stages, the control voltage input effectively introduces an offset voltage into the Ci,Ci' input of amount

$$V_{OS} = \frac{k}{(1-k)}(V_c - V_{c'}) \tag{12-4}$$

where k is a fraction between 0 and 1 and is usually 0.5 or less. As shown in the waveforms of Figure 12-52(d), if the input Ci,Ci' has a duty factor other than 50% and the rise and fall times are sufficiently long, we can dial in an offset voltage that will bring the output of the corrector stage to 50% duty factor.

The voltage generator in Figure 12-52(b) is a differential stage whose outputs are loaded with large capacitors (usually FETs). If the time constant $R_{load} \cdot C_{load}$ is

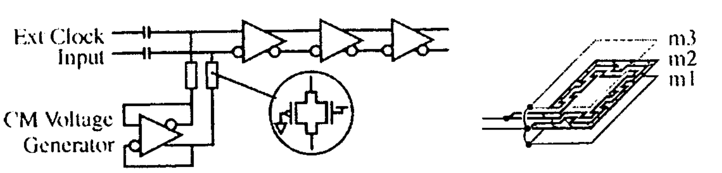
much larger than the period of the waveform on Cc,Cc', the differential voltage between outputs $V_c, V_{c'}$ is proportional to the duty factor of Cc,Cc'. If the voltage generator is connected in a feedback loop around the corrector stage, as shown in Figure 12-52(c), the feedback tends to pull Cc,Cc' toward a 50% duty factor.

Practical considerations for designing a duty-factor corrector include ensuring small (slow) enough edge slopes that the corrector has something to work with (sinusoidal inputs work well with correctors) and obtaining sufficient feedback gain that the control voltage has enough "authority" over the corrected outputs. The feedback gain is adjustable through k but, as k is made larger, less of the corrector stage's gain is available to the signal input, and the output swing limits will become strong functions of the control voltage. A follow-on stage may be needed to "clean up" the swing offset in the Cc,Cc' outputs.

12.2.4.4 Clock Input Conditioning

A DLL receives its reference clock from a source whose signal swing and common-mode voltage generally are different from the "native" signal swing of the delay elements inside the delay line. The difference between the internal common-mode voltage and that of the external signal is amplified by the common-mode gain of the first stage. The common-mode gain is less than unity and is inverting, and thus the output swing of the first stage is generally closer to, but still not equal to, the native signal swing. This effect may persist for a few stages into the delay line, reduced at each stage by the (fractional) common-mode gain, and it is coupled through load imperfections into the timing of the differential signal crossings, thus introducing systematic jitter into the delay line.

This effect can be avoided, and the common-mode input range greatly extended, by AC coupling and DC restoration of the input clock, as shown in Figure 12-53(a). A common-mode voltage reference generator can be built using a copy of a typical delay stage with inputs shorted to outputs. Input capacitors are charged to the difference between internal and external common-mode voltages through resistors, which may be implemented, for example, with permanently on pass gates implemented with long-channel FETs. Linear capacitors should be used for this purpose. A suitable capacitor can be constructed from multiple levels of metal interconnect, thus taking best advantage of both plate and fringing capacitances, as sketched in Figure 12-53(b). The input capacitors and resistors form a high-pass filter whose cutoff frequency should be set well below the lowest frequency of the external clock.



(a) Capacitor Coupling/DC Restoration (b) Linear Capacitor Layout

FIGURE 12-53 Clock Input Conditioning